IN THE CLAIMS

Please amend claims 1-6 and 9-20 in accordance with the following listing showing the status of all claims in the application.

1. (Currently Amended) A method of generating synthesis ~~scripts~~script to synthesize an integrated circuit (IC) ~~designs~~design from a ~~generic netlist~~RTL code description into a gate-level description, said method comprising the steps of:

causing a logic synthesis tool to generate a generic netlist from the RTL code description;

identifying hardware elements in the generic netlist;

determining key pins for each of said identified hardware elements;

extracting design structure and design hierarchy from the ~~Generic~~generic netlist~~;~~ based on the key pins and the identified hardware elements; and

generating script to cause a~~t~~he logic synthesis tool to ~~apply bottom-up synthesis to modules and sub-modules of the IC design;~~synthesize the IC design into a gate-level description based on the design structure and the design hierarchy extracted from the generic netlist,

~~generating~~wherein said script includes instructions to cause a~~t~~he logic synthesis tool to:

apply ~~top-down characterization~~bottom-up synthesis to modules and sub-modules of the IC design~~; and~~,

apply top-down characterization to modules and sub-modules of the IC design, and

repeat said bottom-up synthesis and said top-down characterization until constraints are satisfied.

~~generating script to cause a logic synthesis tool to repeat said bottom-up and said top-down applications until constraints are satisfied.~~

2. (Currently Amended) A The method according to claim 1 wherein said step of extracting design structure allows for a multilevel structuring of modules of the IC design.

3. (Currently Amended) A The method according to claim 1 ~~further comprising the step of generating~~ wherein the script ~~to cause a~~ also causes the logic synthesis tool to apply an initial mapping to the IC design.

4. (Currently Amended) A The method according to claim 1 wherein the logic synthesis tool is Synopsys Design Compiler.

5. (Currently Amended) A The method according to claim 1 further comprising the step of rearranging the design hierarchy ~~by changing~~ of the IC design.

6. (Currently Amended) A The method according to claim 1 ~~further comprising the step of generating~~ wherein the script ~~to cause a~~ also causes the logic synthesis tool to ungroup modules of the IC design.

7. (Canceled)

8. (Canceled)

9. (Currently Amended) An apparatus for generating synthesis ~~scripts~~script to synthesize an integrated circuit (IC) ~~designs in~~design from a RTL ~~level~~code description into a gate-level description, comprising:

a processor;

memory connected to said processor;

said memory having instructions for said processor to :

~~determine key pins for identified hardware elements from~~cause a logic synthesis tool to generate a generic netlist from the RTL code description;

~~extract critical design structure and hierarchy from~~identify hardware elements in the generic netlist;

determine key pins for each of said identified hardware elements;

extract design structure and design hierarchy from the generic netlist based on the key pins and the identified hardware elements; and

generate script to cause the logic synthesis tool to synthesize the IC design into a gate-level description based on the design structure and the design hierarchy extracted from the generic netlist,

wherein said script includes instructions to cause the logic synthesis tool to:

apply bottom-up ~~synthesis to~~ synthesis to modules and sub-modules ~~of the IC design;~~ of the IC design,

apply top-down characterization to modules and sub-modules of the IC design~~;~~

~~repeat said bottom-up and said top-down applications~~, and

repeat said bottom-up synthesis and said top-down characterization until constraints are satisfied~~; and~~

~~create design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.~~.

10. (Currently Amended) An apparatus for generating synthesis ~~scripts~~script to synthesize an integrated circuit (IC) ~~designs in~~design from a RTL ~~level~~code description into a gate-level description, comprising:

means for ~~determining key pins for identified hardware elements from~~causing a logic synthesis tool to generate a generic netlist from the RTL code description;

means for ~~extracting critical design structure and hierarchy from~~identifying hardware elements in the generic netlist;

means for ~~applying bottom-up synthesis to modules and sub-modules of the IC design;~~

~~means for applying~~determining key pins for each of said identified hardware elements;

means for extracting design structure and design hierarchy from the generic netlist based on the key pins and the identified hardware elements; and

means for generating script to cause the logic synthesis tool to synthesize the IC design into a gate-level description based on the design structure and the design hierarchy extracted from the generic netlist,

wherein said script includes instructions to cause the logic synthesis tool to:

apply bottom-up synthesis to modules and sub-modules of the IC design,

apply top-down characterization to modules and sub-modules of the IC design~~;~~

~~means for repeating said bottom-up and said top-down applications~~, and

repeat said bottom-up synthesis and said top-down characterization until constraints are satisfied~~; and~~

~~means for creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.~~.

11. (Currently Amended) A computer storage medium containing instructions for generating synthesis ~~scripts~~script to synthesize an integrated circuit (IC) ~~designs in RTL level description into~~design from a generic netlist into a gate-level description, said instructions comprising the steps of:

causing a logic synthesis tool to generate a generic netlist from the RTL code description;

identifying hardware elements in the generic netlist;

determining key pins for each of said identified hardware elements;

extracting ~~critical~~ design structure and design hierarchy from the generic netlist~~;~~ based on the key pins and the identified hardware elements; and

~~applying bottom-up synthesis to modules and sub-modules of the IC design;~~generating script to cause the logic synthesis tool to synthesize the IC design into a gate-level description based on the design structure and the design hierarchy extracted from the generic netlist,

~~applying top-down characterization to modules and sub-modules of the IC design;~~wherein said script includes instructions to cause the logic synthesis tool to:

apply bottom-up synthesis to modules and sub-modules of the IC design,

apply top-down characterization to modules and sub-modules of the IC design, and

repeat said bottom-up synthesis and said top-down characterization until constraints are satisfied.

~~repeating said bottom-up and said top-down applications until constraints are satisfied; and~~

~~creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.~~

12. (Currently Amended) AThe computer storage medium of claim 11 wherein said computer storage medium is selected from a group consisting of magnetic device, optical device, magneto-optical device, floppy diskette, CD-ROM, magnetic tape, computer hard drive, and memory card.

13. (Currently Amended) A process for ~~generating synthesis scripts to synthesize~~synthesizing an integrated circuit (IC) ~~designs in~~design from a RTL ~~level~~code description into a gate-level description, said process comprising the steps of:

generating a generic netlist from the RTL code description;

identifying hardware elements in the generic netlist;

determining key pins for ~~each of said~~the identified hardware elements in the generic netlist;

extracting ~~critical~~ design structure and design hierarchy from the generic netlist based on the identified hardware elements and the key pins;

~~applying bottom-up synthesis to modules and sub-modules of the IC design;~~

synthesizing the IC design into a gate-level description based on the design structure and the design hierarchy extracted from the generic netlist,

~~applying top-down characterization to modules and sub-modules~~wherein said synthesis of the IC design~~;~~ includes:

applying bottom-up synthesis to modules and sub-modules of the IC design,

applying top-down characterization to modules and sub-modules of the IC design, and

repeating said bottom-up synthesis and said top-down characterization until constraints are satisfied.

~~repeating said bottom-up and said top-down applications until constraints are satisfied; and~~

~~creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.~~

14. (Currently Amended) A computer system for ~~generating synthesis scripts to synthesize~~synthesizing an integrated circuit (IC) ~~designs in~~design from a RTL ~~level~~code description into a gate-level description, said system comprising:

means for generating a generic netlist from the RTL code description;

means for identifying hardware elements in the generic netlist;

means for determining key pins for the identified hardware elements ~~from a~~in the generic netlist;

means for extracting ~~critical~~ design structure and design hierarchy from the generic netlist based on the identified hardware elements and the key pins;

means for ~~applying bottom-up synthesis to modules and sub-modules of the IC design;~~synthesizing the IC design into a gate-level description based on the design structure and the design hierarchy extracted from the generic netlist,

~~means for applying top-down characterization to modules and sub-modules~~wherein said synthesis of the IC design~~;~~ includes:

applying bottom-up synthesis to modules and sub-modules of the IC design,

applying top-down characterization to modules and sub-modules of the IC design, and

repeating said bottom-up synthesis and said top-down characterization until constraints are satisfied.

~~means for repeating said bottom-up and said top-down applications until constraints are satisfied; and~~

~~means for creating design compile scripts to synthesize modules and sub-modules and the IC design having said satisfied constraints.~~

15. (Currently Amended) AThe method according to Claim 1, wherein I/O conditions and I/O constraints of the modules of the IC design are captured during the top-down characterization and are used to re-optimize the IC design during the bottom-up synthesis.

16. (Currently Amended) AThe computer storage medium according to Claim 11, wherein I/O conditions and I/O constraints of the modules of the IC design are

captured during the top-down characterization and are used to re-optimize the IC design during the bottom-up synthesis.

17. (Currently Amended) ~~A~~The process according to Claim 13, wherein I/O conditions and I/O constraints of the modules of the IC design are captured during the top-down characterization and are used to re-optimize the IC design during the bottom-up synthesis.

18. (Currently Amended) ~~An~~The apparatus according to Claim 9, wherein I/O conditions and I/O constraints of the modules of the IC design are captured during the top-down characterization and are used to re-optimize the IC design during the bottom-up synthesis.

19. (Currently Amended) ~~An~~The apparatus according to Claim 10, wherein I/O conditions and I/O constraints of the modules of the IC design are captured during the top-down characterization and are used to re-optimize the IC design during the bottom-up synthesis.

20. (Currently Amended) ~~A~~The computer system according to Claim 14, wherein I/O conditions and I/O constraints of the modules of the IC design are captured

during the top-down characterization and are used to re-optimize the IC design during the bottom-up synthesis.